INTERNATIONAL STANDARD

ISO/IEC 18372

First edition
2004-12

Information technology –

RapidIO™ interconnect specification

PRICE CODE XJ

For price, see current catalogue

Table of Contents

Table of Contentss

Table of Contents

Table of Contentss

Table of Contents

Table of Contentss

Table of Contents

Table of Contentss

Table of Contents

Table of Contentss

Table of Contents

Table of Contentss

Table of Contents

List of Figures

Partition I - Input/Output Logical Specification

Partition II - Message Passing Logical Specification

List of Figures

Partition III - Common Transport Specification

Partition IV - Physical Layer 8/16 LP-LVDS Specification

List of Figures

Partition V - Globally Shared Memory

List of Figures

Partition VI - Physical Layer 1x/4x LP-Serial Specification

List of Figures

Partition VII - Interoperability Specification System and Device

Partition VIII - Error Management Extentions Specification

List of Tables

Partition I - Input/Output Logical Specification

Partition II - Message Passing Logical Specification

List of Tables

Partition III - Common Transport Specification

Partition IV - Physical Layer 8/16 LP-LVDS Specification

List of Tables

Partition V - Globally Shared Memory

List of Tables

Partition VI - Physical Layer 1x/4x LP-Serial Specification

List of Tables

Partition VII - Interoperability Specification System and Device

Partition VIII - Error Management Extentions Specification

List of Tables

INFORMATION TECHNOLOGY – RAPIDIO™ INTERCONNECT SPECIFICATION

FOREWORD

1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

3) All users should ensure that they have the latest edition of this publication.

4) No liability shall attach to IEC or ISO or its directors, employees, servants or agents including individual experts and members of their technical committees and IEC or ISO National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this ISO/IEC publication or any other IEC or IEC/ISO publications.

5) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.

6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

International Standard ISO/IEC 18372 was developed by ECMA International (as ECMA-342) and was adopted, under a special “fast-track procedure”, by ISO/IEC joint technical committee 1: Information technology (ISO/IEC JTC 1), in parallel with its approval by national bodies of ISO and IEC. It has been added to the programme of work of subcommittee 25: Interconnection of information technology equipment, of ISO/IEC JTC 1.

INTRODUCTION

The RapidIO™ architecture was developed to address the need for a high-performance low pin count packet-switched system level interconnect to be used in a variety of applications as an open standard. The architecture is targeted toward networking, telecom, and high performance embedded applications. It is intended primarily as an intra-system interface, allowing chip-to-chip and board-to-board communications at Gigabyte per second performance levels. It provides a rich variety of features including high data bandwidth, low-latency capability and support for high-performance I/O devices, as well as providing globally shared memory, message passing, and software managed programming models. In its simplest form, the interface can be implemented in a FPGA end point. The interconnect defines a protocol independent of a physical implementation. The physical features of an implementation utilizing the interconnect are defined by the requirements of the implementation, such as I/O signaling levels, interconnect topology, physical layer protocol, error detection, and so forth. The architecture is intended and partitioned to allow adaptation to a multitude of applications.

Overview of the standard

This overview explains each of the three layers of the RapidIO architecture, their interrelationships, an the system and device interoperability:

1. Logical layer—The logical layer defines the overall protocol and packet formats, the types of transactions that can be carried out with RapidIO, how addressing is handled. The logical specifications are partitioned into three partitions:

   — *Partition I: Input/Output Logical Specification*

   — *Partition II: Message Passing Logical Specification*

   — *Partition V: Globally Shared Memory Logical Specification*

2. Transport layer—The transport layer provides the necessary route information for a packet to move from one point to another. This information is covered in *Partition III: Common Transport Specification.*

3. Physical layer—The physical layer contains the device level interface such as packet transport mechanisms, flow control, electrical characteristics, and low-level error management. This standard covers these topics in *Partition IV: Physical 8/16 LP-LVDS Specification,* and in *Partition VI: Physical Layer 1X/4X LP-Serial Specification.*

4. Interoperability — This consists of a standard set of device and system design solutions to provide for interoperability. The specification is given in *Patition VII: Interoperability Specification System and Device.*

NOTE

RapidIO specifications are structured so that additions can be made to each without affecting the others. For example, each logical specification is independent and can be implemented alone.